Lodz University of Technology
Institute of Physics

Laboratory of electronics

Exercise E14IFE

Digital logic components

Version 1.1 (11 April 2018)

Table of contents:

Before you start to perform an experiment you are obliged to have mastered the following theoretical subjects:

1. Definition of high and low logic states for TTL and CMOS logic circuits. [1-3,6]
2. Description of static properties of logic gates. The most important characteristics and parameters. [1-4]
3. What is DC noise immunity of logic gates? [1,2,6]
4. Graphic symbols of basic logic gates: AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR, and buffet gate. [1-5]
5. Comparison of internal structure of NAND gates of TTL and CMOS family. [1-5]

1. Purpose of the exercise

The purpose of this experiment is to investigate the static input, transfer, and output characteristics of a TTL logic gate.

2. Hazards

Type	Absence	Low	Medium	High
electrical radiation hazards		+		
optical radiation hazards	+			
mechanical hazards (including acoustic hazards, noise)	+			
electromagnetic radiation hazards (invisible)	+			
biological hazards	+			
ionizing radiation hazards	+			
chemical hazards	+			
thermal hazards (including explosion and fire)	+			

The cables with banana plugs are designed exclusively for use in low-voltage circuits - do not connect them to the mains supply 230 V.

3. Introduction

Integrated circuits made in TTL technology (Transistor-Transistor Logic) was the first widely-used class of digital circuits and become the basis for building computers and other digital electronics. At present other technologies are used to build very-large-scale integrated circuits, however, TTL devices are still used as “glue” logic.

TTL digital circuits are built from bipolar junction transistors and resistors, and powered by a DC voltage of 5 V. The fundamental logic gate of the TTL family is the NAND gate, in which the inputs are connected directly to the emitters of a multiple-emitter transistor (Fig. 1). This structure is functionally equivalent to multiple transistors where the bases and

collectors are tied together. Moreover, transient-voltage-suppression diodes are used to protect transistor from voltage spikes induced on connected wires.

Let us consider in more detail the operation of the circuit shown in Fig. 1. When both inputs are at logic "1" state (close to the supply voltage +5 V) the base-emitter junctions of transistor T1 are reverse biased. This allow current to flow through the base-collector junction of T1 to the base of T2, causing T2 to saturate. The collector voltage of T2 falls to almost zero, therefore T3 is off. Some of the emitter current of T2 flows into the base of T4 turning it on, consequently the output Y falls to about +0.2 V, which corresponds to "0" logic state.

If any of the inputs is at "0" the current (with a typical value of about 1 mA) flows to this input through the base-emitter junction of T1, making the base of T1 low. As a result T2 is off and the resistor 1,6 kΩ pull up its collector voltage, causing T3 to be turned on. The output is taken from the emitter of T3 (emitter follower mode) and so the voltage of the output Y will be not less than +3.3 V, which corresponds to a logical "1".

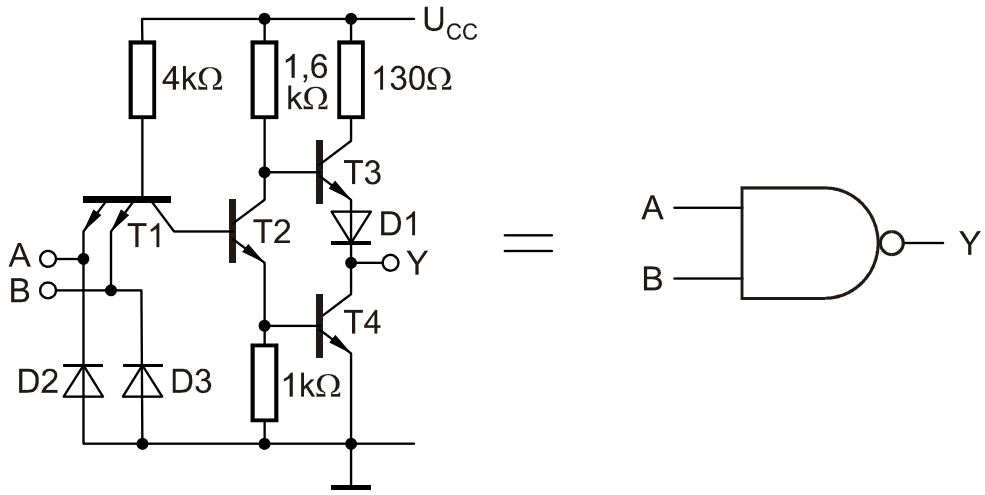

Fig. 1. Internal structure of a two-inputs standard TTL NAND gate.

In this experiment a single logic NOT gate from TTL family will be investigated. Since several logic NOT gates are placed in a single chip, a UCY 7430 chip with one 8-input NAND gate is applied. Such approach allows you to measure supply current I_s of the single gate without perturbation cased by another gates in the same chip. On the front panel of the experimental kit only one input of the NAND gate is brought out, while the others are always held in high state.

4. Available equipment

4.1. Experimental module

The front panel of experimental module is shown in Fig. 2. The module consists of four functional blocks:

a) the potentiometer P_1 working as a voltage divider, which allows you to adjust an input voltage in the range from 0 to 5 V,
b) NOT logic gate,

c) the potentiometer P_2 working as a resistive load, which allows you to adjust an output current in the range from 0 to about 15 mA (slightly less than the maximum static output current given in TTL data sheet),
d) alternative load of the output of the gate in the form of inputs of further logic gates, where the number of inputs may be selected in the range from 1 to 12.

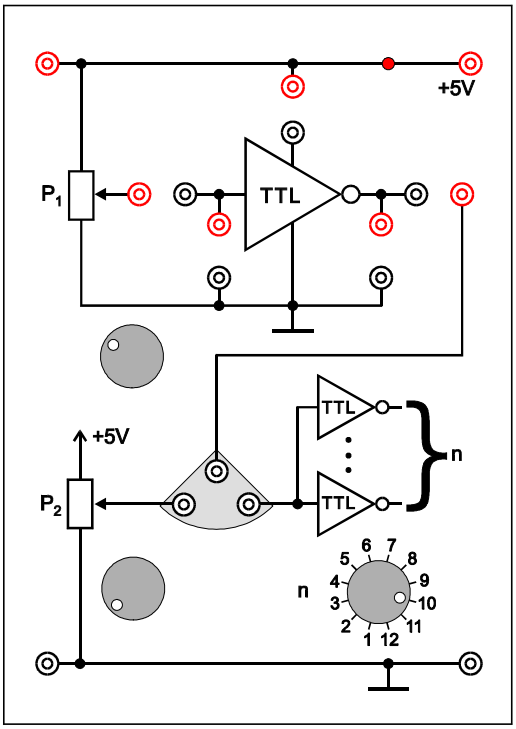

Fig. 2. The front panel of experimental module.

4.2. Multimeters

The voltages and currents in the experimental module will be measured using three digital multimeters. The following models may be used: KT890, M-3800, M-4650, UT-804 or Protek 506 [7].

4.3. Power supply

The experimental module is powered by the laboratory power supply SIGLENT SPD3303D [7]. In this experiment, only the channel that provides constant output voltage +5 V is used.

4.4. Function generator

A function generator DF1641B [7] is used as a source of TTL compatible square wave.

4.5. Oscilloscope

In this experiment, two-channel analogue oscilloscope GOS-620 or GOS-630 [7] is used.

5. Experimental procedure

5.1. Input characteristic of a logic gate (basic version)

1. Connect the power supply (Z – SPD3303D), milliammeter (mA), voltmeter (V) and jumper to the experimental module with logic gate as shown in Fig. 3.
   WARNING:
   a) the experimental module must be supplied from the power supply channel that provides constant output voltage +5 V (sockets on the right side of the power supply). Do not use the outputs allowing voltage adjustment,
   b) do not connect +5 V voltage output directly to the output nor input of the gate.
   Ignoring these recommendations threatens to damage the device.
2. Select the best measuring range of the ammeter (mA) for currents up to 1 mA DC (range 2 mA DC for KT890, M-3800 and M-4650, auto range or a range 40 mA DC for UNI-T UT804, whereas the multimeter Protek 506 is not recommended for this measurement because of the lack of the appropriate measuring range).
3. Select the best measuring range of the voltmeter (V) for voltages up to 5 V DC (range 20 V DC for KT890, M-3800 and M-4650, auto range or a range of 40 V DC for Protek 506 and UNI-T UT804 multimeters).
4. After obtaining permission from your supervisor switch on power supply. Check out the status of the red LED located on the +5 V line in the experimental module.
5. Use the potentiometer P_1 to change the voltage U_{in} on the input of the NOT gate from 0 to 5 V and determine the dependency of the input current I_{in} on U_{in}. Special attention should be paid to measure U_{in} in the range $1.3 \div 1.6$ V, where small changes in U_{in} may cause sudden changes in I_{in}. Write down the results in Table 1.
6. Switch off the power supply and disconnect the circuit.

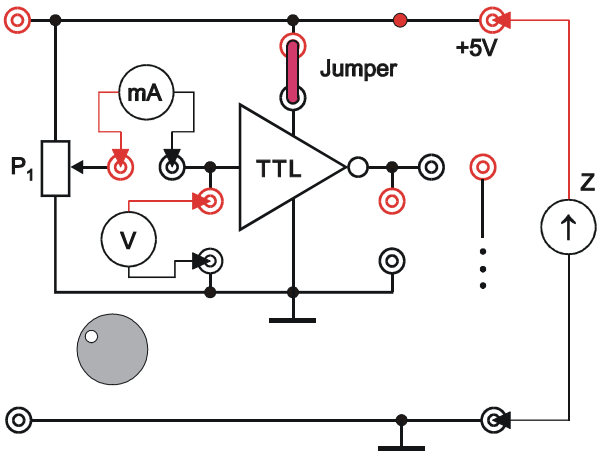

Fig. 3. Setup for measuring input characteristic of a logic gate.

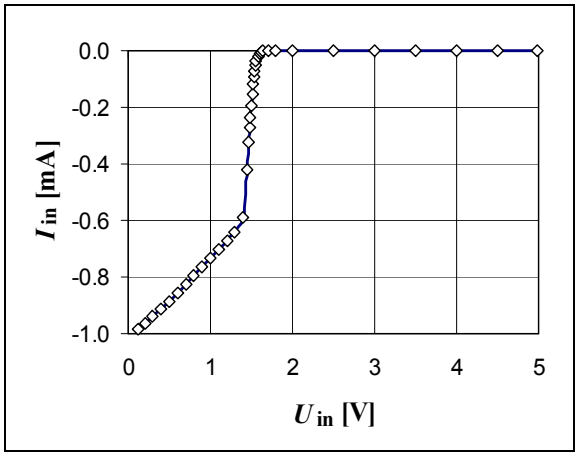

Fig. 4. Typical input characteristic of a TTL logic gate.

#	U_{in} [V]	I_{in} [mA]
1		
2		

Table 1. Data table for measurements of input characteristic of the logic gate.

5.2. Transfer characteristic and power dissipation of a logic gate (basic version)

1. Connect the circuit shown in Fig. 5. Select the best measuring range of the ammeter (mA) for currents up to 15 mA DC and the best measuring range of the voltmeters (V1) and (V2) for voltages up to 5 V DC.
2. After obtaining permission from your supervisor switch on power supply.
3. If the supervisor did not recommend any other settings, use the rotary switch "n" to select a load of the gate output by $n = 10$ inputs of further logic gates.
4. Use the potentiometer P_1 to increase the input voltage U_{in} from 0 to 5 V and determine the dependency of the output voltage U_{out} and quiescent supply current I_s on U_{in}. Special attention should be paid to measure U_{in} in the range 1.2 ÷ 1.5 V, where small changes in U_{in} may cause sudden changes in U_{out} and I_s. Write down the results in Table 2.
5. Switch off the power supply and disconnect the circuit.

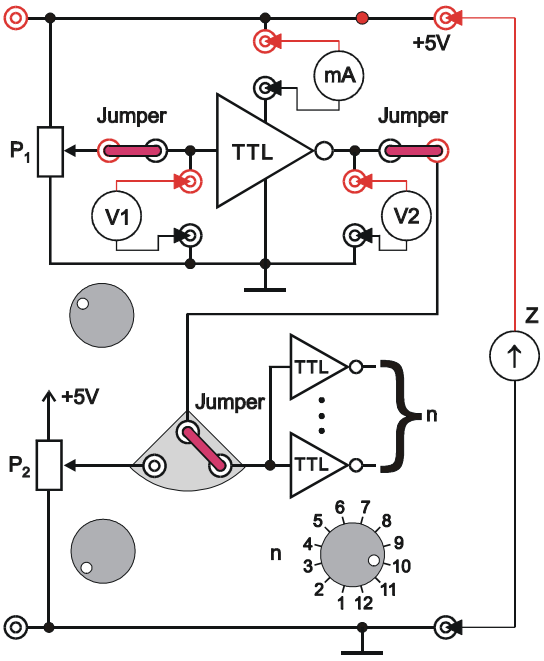

Fig. 5. Setup for measuring transfer characteristics and quiescent supply current of a logic gate.

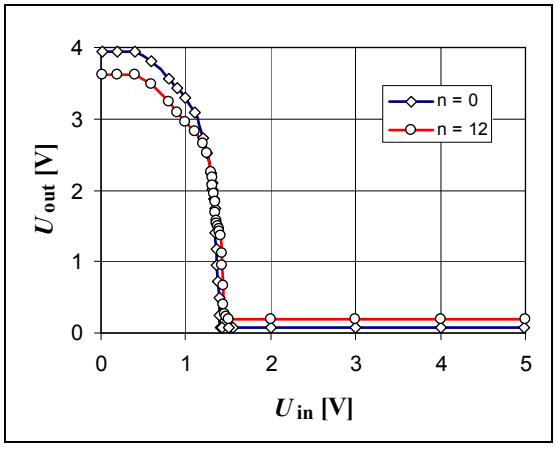

Fig. 6. Typical transfer characteristics of a TTL inverter.

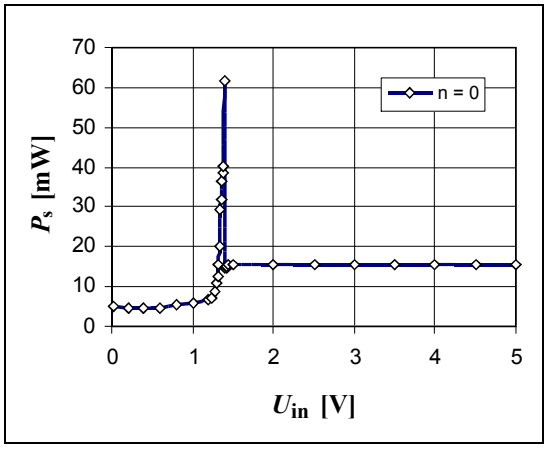

Fig. 7. Typical power dissipation of a TTL logic gate versus input voltage.

#	n = …			
	U_{in} [V]	U_{out} [V]	I_s [mA]	P_s [mW]

Table 2. Data table for measurements of transfer characteristics and power dissipation of the logic gate.

5.3. Output characteristic of a logic gate (basic version)

1. Connect the circuit shown in Fig. 8. Select the best measuring range of the ammeter (mA) for currents up to 15 mA DC and the best measuring range of the voltmeter (V) for voltages up to 5 V DC.
2. After obtaining permission from your supervisor switch on power supply.
3. Turn the potentiometer P_1 fully counter clock-wise to set the low state at the gate input.
4. Use the potentiometer P_2 to change the output current $I_{out,H}$ in the entire available range (from 0 to about 15 mA) and determine the dependency of the output voltage $U_{out,H}$ on $I_{out,H}$ for the high state at the gate output. Write down the results in Table 3.
5. Turn the potentiometer P_1 fully clock-wise to set the high state at the gate input. Repeat the procedure described in step 3 and write down the results $U_{out,L}$ and $I_{out,L}$ related to the low state at the output.
6. Switch off the power supply and disconnect the circuit.

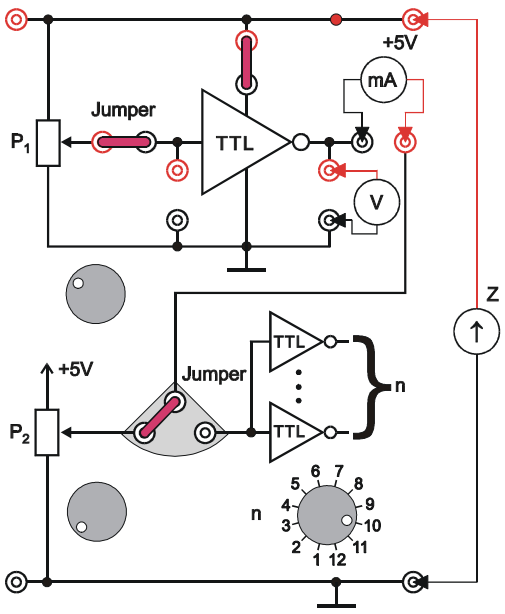

Fig. 8. Setup for measuring output characteristics of a logic gate for the resistive load.

#	the high output state		the low output state	
	$I_{out,H}$ [mA]	$U_{out,H}$ [V]	$I_{out,L}$ [mA]	$U_{out,L}$ [V]
1				
2				

Table 3. Data table for measurements of output characteristic of the logic gate for the resistive load.

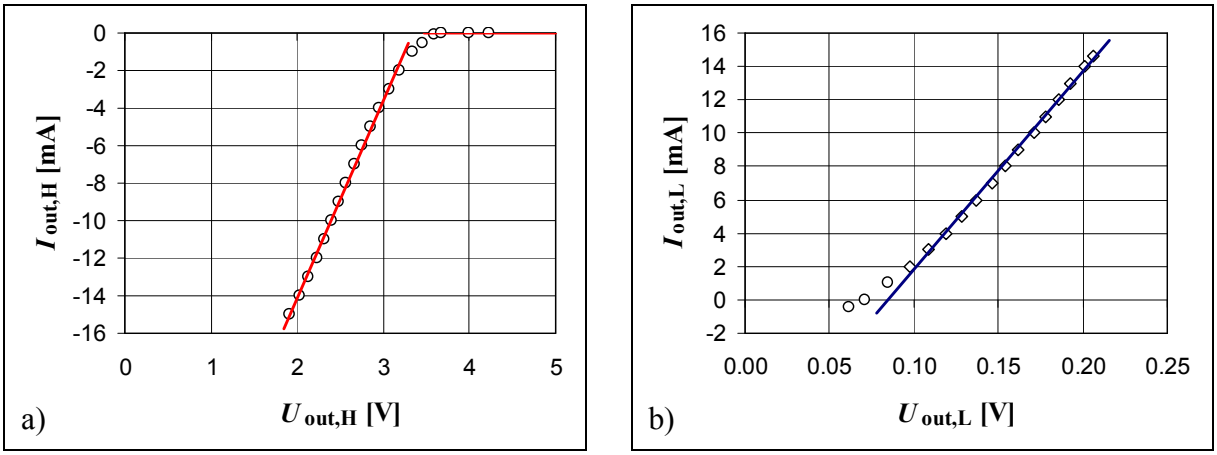

Fig. 9. Typical output characteristics of a TTL logic gate for a resistive load. a) the high output state, b) the low output state.

5.4. Visualization of transfer characteristic of a logic gate (extended version)

1. Connect the function generator (G), oscilloscope (U_X i U_Y) and power supply (Z) with the logic gate as shown in Fig. 10. Pay attention to the fact that the signal must be taken from the universal OUTPUT of the generator, not the digital TTL OUT. Use the BNC T-adapter to bring the signal from the function generator to the CH1 input of the oscilloscope and to the input of the logic gate.
2. Set the function generator's amplitude to a minimum.
3. After obtaining permission switch on the generator, oscilloscope and power supply.
4. Set the function generator to give a triangle waveform of about 1 kHz. Select the channel CH1 on the oscilloscope and GND coupling mode. Then adjust the vertical position of the ground (zero volt) level to align it with the vertical grid line on the bottom of the screen. Select the DC coupling mode in the CH1 channel. Press the DC OFFSET button on the function generator to turn on the DC component of the waveform at the output and adjust the DC voltage and amplitude to obtain a signal varying between 0 V and 5 V.
5. Set the oscilloscope to X-Y mode. In order to use the entire screen area it is recommended to set the (0, 0) point in the lower left corner of the screen.
6. Use the rotary switch “n” in the experimental module to select a load of the gate output the same as before in section 5.2. Copy the characteristic from the oscilloscope's screen, write down the V/DIV sensitivity for the X and Y inputs.
7. Repeat the observation for any other load of the gate output.
8. Switch off the power supply and disconnect the circuit.

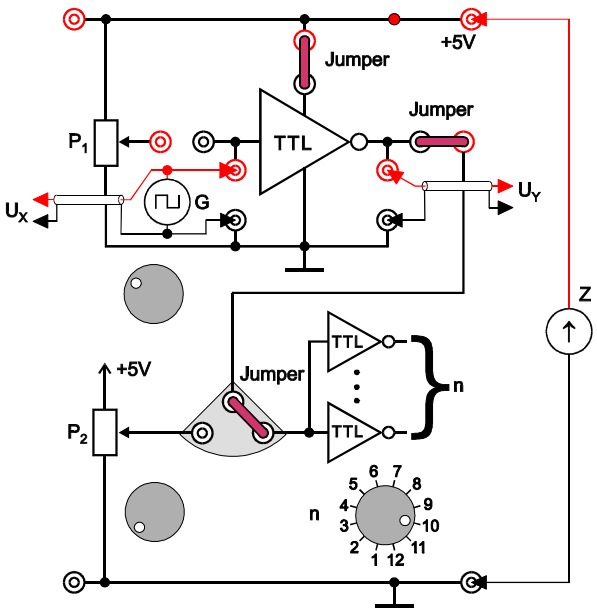

Fig. 10. Setup for visualization of transfer characteristics of a logic gate.

6. Report elaboration

Report has to be composed of:

1. Front page (by using a pattern).
2. Description of experiment purposes.
3. Basic definitions, formulas, description of used marks and symbols.
4. Schematic diagrams of tested circuits.
5. List of used instruments and devices (id number, type, setting and range values).
6. Measuring results.
7. Plots, calculations, analysis, interpretation and sub-conclusions related to all required points of "Experimental procedure". In particular:
   - 7.1. Use the obtained results to plot the input characteristic $I_{in} = f_1(U_{in})$ for the investigated logic gate. Check out if the maximum number (16 mA /$I_{in,max}$) of driven inputs of gates is greater than the catalog value of 10, which includes a certain reserve for dispersion of parameters and growth of power dissipation at higher frequencies. $I_{in,max}$ is the maximum absolute value of input current read from your plot and 16 mA is the maximum permitted output current for standard TTL gate.
   - 7.2. Plot the transfer characteristic $U_{out} = f_2(U_{in})$ for the selected number n of the inputs of driven gates. Find in the literature the voltage ranges assumed to represent the low (logical 0), high (logical 1), and unknown logic states at inputs of TTL digital circuits. Check out if a given logic gate correctly transpose the entire voltage range corresponding to the low state at the input to the high state at its output and the entire range for high state at the input to the low state at the output. If so, calculate DC noise immunity (here DC means the long-lasting signals in comparison to the propagation time through a gate). Low level DC noise immunity may be found as the difference $U_{IL} - f_2(U_{IH})$, where U_{IL} is the boundary voltage between the low and unknown logic states defined for a TTL input signals, U_{IH} is the boundary between the high and unknown logic states, and $f_2(U_{IH})$ is the response of a given logic gate for the U_{IH} input voltage. High level DC noise immunity is given by the formula

$f_2(U_{IL}) - U_{IH}$. The smaller of these two differences is DC noise immunity guaranteed for any state. In order to ensure correct transmission of a logic state from the output to the input of next gate, DC noise immunity must be higher than the disruptions in transmission line.

7.3. Calculate the power dissipated in the gate $P_s = U_s I_s$, where I_s is the measured supply current and $U_s = 5$ V is the supply voltage. Plot the calculated power versus the input voltage $P_s = f_3(U_{in})$.

7.4. Plot the output characteristics $I_{out} = f_4(U_{out})$ of the investigated gate separately for the low and high output states. Based on your graphs, determine whether there exists a boundary output current, which leads to unknown logic state at the output when the input has any determinated state.

7.5. Calculate differential output resistances $\partial U_{out} / \partial I_{out}$ of the gate for the low and high output states. In calculations ignore all data that have a bad fit to the linear trends at the plots made in previous step. Do not find differential resistance taking only two selected measuring points! To improve the accuracy of your calculations use the least square method to find the slope of the straight lines at the output characteristics. The differential resistance is reciprocal of the slope.

7.6. Compare the transfer characteristics obtained using the oscilloscope with the characteristics resulting from the "point by point" method. Discuss the consistency of the results.

8. Remarks and final conclusions.

The report will be evaluated for the language, completeness, correctness, clarity of presentation of the results (in the form of tables, graphs, oscillograms and results of calculations together with descriptions) and quality of discussion and conclusions. All of the components listed above will be evaluated in the report. Theoretical introduction is not required and is not included in the assessment.

7. References

7.1. Basic reference materials

[1] J. Kalisz, *Podstawy elektroniki cyfrowej*, WKiŁ, Warszawa 2002.
[2] W. Marciniak, *Przyrządy półprzewodnikowe i układy scalone. Zasady działania, technologia i zastosowania*, WNT, Warszawa 1979.
[3] P. Horowitz, W. Hill, *Sztuka elektroniki*, WKiŁ, Warszawa 2001,
[4] A. Rusek, *Podstawy elektroniki*, część 2, Wydawnictwa Szkolne i Pedagogiczne, Warszawa, 1983.
[5] U. Tietze, Ch. Schenk, *Układy półprzewodnikowe*, WNT, Warszawa 1987.
[6] A. Charoy, *Zakłócenia w urządzeniach elektronicznych*, tom 1, WNT, Warszawa 1999.

7.2. Other reference materials

[7] User guides for multimeters, power supply, function generator, and oscilloscope available on the website:
https://fizyka.p.lodz.pl/pl/dla-studentow/fundamentals-of-electronics/